IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.(Currently Amended) ~~Circuit~~ A circuit for driving a load, comprising:

[[-]] two input terminals ~~(11,12)~~ for connection to a source of a supply voltage ~~(V_{sup})~~;

[[-]] a first output terminal and a second output terminal ~~(26, 27)~~ for connection to the load ~~(4)~~;

[[-]] at least one inductor ~~(28)~~ coupled between one of the output terminals and a corresponding connection node ~~(15)~~;

[[-]] at least one arrangement ~~(80)~~ comprising a switch ~~(M1)~~ coupled between one of said input terminals ~~(11)~~ and one of said connection nodes ~~(15)~~, a diode ~~(D1)~~ being connected between said one connection node and the other input terminal ~~(12)~~;

[[-]] a control unit for controlling said ~~one or more switches (M1, M2)~~ switch;

~~characterized in that each~~ wherein said at least one arrangement ~~(80)~~ and a corresponding diode ~~(D1)~~ are designed to allow the voltage over ~~the~~ an opened switch ~~(M1)~~ of said at least one arrangement to return to substantially zero before said opened switch ~~(M1)~~ is closed, the control unit being designed to provide a signal for closing the opened switch ~~(M1)~~ when a substantially zero voltage over said opened switch ~~(M1)~~ is detected.

2.(Currently Amended) ~~Circuit according to claim 1~~ A circuit for driving a load ~~(4)~~ with a substantially square wave current, comprising:

a first input terminal and a second input for connection to a source of a supply voltage;

a first output terminal and a second output terminal for connection to the load;

at least one inductor coupled between one of the first output terminal and the second output terminal and a corresponding connection node;

[[-]] a first arrangement ~~(80)~~ comprising a first switch ~~(M1)~~ coupled between the first input terminal ~~(11)~~ and ~~one of the~~

~~said~~ a first connection ~~nodes (15)~~ node, and a first diode ~~(D1) being~~ connected between said ~~one~~ first connection node ~~(15)~~ and the second input terminal ~~(12)~~;

[[-]] a second arrangement ~~(81)~~ comprising ~~the~~ a second switch ~~(M2)~~ coupled between the second input terminal ~~(12)~~ and ~~one of the said~~ a second connection ~~nodes (15, 16)~~ node, and a second diode ~~(D2) being~~ connected between said ~~one~~ second connection node ~~(15,16)~~ and the first input terminal ~~(11)~~; and

a control unit for controlling said first switch and said second switch;

wherein said first arrangement and said second arrangement are designed to allow a voltage over an opened switch of said first arrangement and said second arrangement to return to substantially zero before said opened switch is closed, the control unit being designed to provide a signal for closing the opened switch when a substantially zero voltage over said opened switch is detected; and

[[-]] wherein the control unit ~~being~~ is further designed to generate ~~its~~ control signals in commutation intervals ~~(30, 31)~~, said first switch ~~(M1)~~ being operated during a first interval ~~(30)~~ causing a load current having substantially a first direction, and

said second switch ~~(M2)~~ being operated during a second interval ~~(31)~~ causing a load current having substantially ~~the~~ a second direction which is opposite the first direction.

3.(Currently Amended) ~~Circuit~~ The circuit according to claim 1, ~~characterized in that~~ wherein said switches ~~(M1,M2)~~ are MOSFET switches.

4.(Currently Amended) ~~Circuit~~ The circuit according to claim 2, ~~characterized in that~~ wherein a first inductor ~~(28)~~ is coupled between ~~an~~ said first output terminal ~~(26)~~ and ~~a~~ said first connection node ~~(15)~~, and a second inductor ~~(29)~~ is coupled between said first output terminal ~~(26)~~ and ~~a~~ said second connection node ~~(16)~~, and wherein the first switch ~~(M1)~~ is coupled between said first connection node ~~(15)~~ and the first input terminal ~~(11)~~ and the second switch ~~(M2)~~ is coupled between said second connection node ~~(16)~~ and the second input terminal ~~(12)~~.

5.(Currently Amended) ~~Circuit~~ The circuit according to claim 2, ~~characterized in that~~ wherein the first arrangement and the

second arrangement each ~~arrangement (80;81)~~ comprises a series connection of a switch ~~(M1; M2)~~ with two diodes coupled in anti-parallel ~~(70,71;72,73)~~, ~~which~~ and wherein the first arrangement and the second arrangement ~~(80,81)~~ are coupled between ~~the~~ respective input terminals ~~(11;12)~~ and a common connection node ~~(15)~~ connected to one side of the inductor ~~(28)~~.

6.(Currently Amended) ~~Circuit~~ The circuit according to claim 2, ~~characterized in that~~ wherein the control unit ~~(20)~~ is further designed to generate a commutation control signal for controlling the commutation intervals ~~(30,31)~~ and a switching signal having a higher frequency than said commutation control signal for controlling ~~the~~ operation of ~~the~~ an active switch, wherein said commutation and said switching signal are synchronized by the control unit ~~(20)~~.

7.(Currently Amended) ~~Circuit~~ The circuit according to claim 6, ~~characterized in that~~ wherein the commutation control signal ensures a commutation from said first interval ~~(30)~~ to said second interval ~~(31)~~ when ~~the~~ a current through the ~~one or more inductors~~

at least one inductor ~~(28, 29)~~ is substantially zero.

8. (Currently Amended) ~~Circuit~~ The circuit according to claim 6, ~~characterized in that~~ wherein the commutation control signal ensures a commutation from said first interval ~~(30)~~ to said second interval ~~(31)~~ when ~~the~~ a current through the at least one inductor ~~(28, 29)~~ is substantially maximum.

Claim 9 (Canceled)

10. (Currently Amended) ~~Control~~ A control unit for use in a circuit ~~according to claim 1, characterized in that~~ for driving a load, the circuit comprising:

two input terminals for connection to a source of a supply voltage;

a first output terminal and a second output terminal for connection to the load;

at least one inductor coupled between one of the output terminals and a corresponding connection node;

at least one arrangement comprising a switch coupled between

one of said input terminals and one of said connection nodes, a diode being connected between said one connection node and the other input terminal;

a control unit for controlling said switch;

wherein said at least one arrangement and a corresponding diode are designed to allow the voltage over an opened switch of said at least one arrangement to return to substantially zero before said opened switch is closed, the control unit being designed to provide a signal for closing the opened switch when a substantially zero voltage over said opened switch is detected;

wherein said control unit comprises:

[[-]] two capacitors coupled in series between one input terminal ~~(12)~~ and one of the connection nodes ~~(15, 16)~~, wherein ~~the~~ a divider node ~~(82,83)~~ between the two capacitors ~~(42,43;40,41)~~ is coupled via a resistor ~~(78;77)~~ to a logic circuit;

[[-]] said logic circuit being designed to provide a signal which turns on the ~~corresponding~~ switch ~~connected to said connection node (15;16)~~ when ~~the~~ a voltage in the divider node ~~(82;83)~~ falls within a predetermined voltage range.

11. (Currently Amended) ~~Control~~ The control unit according to claim 10, ~~characterized in that~~ wherein said logic circuit further comprises a timer ~~(54)~~ which starts running when the active switch ~~(M1;M2)~~ is turned on until a pre-set time period ~~(T_{on})~~ has elapsed, wherein the logic circuit provides a signal for turning off the switch when this pre-set time period has elapsed.

12. (Currently Amended) ~~Control~~ unit according to claim 10, ~~characterized in that~~ wherein said logic circuit further comprises means for detecting a peak current in the load ~~(4)~~, wherein the logic circuit provides a signal for turning off the switch ~~(M1;M2)~~ when said peak current is detected.